What is claimed is:

1. A method of manufacturing a semiconductor device including a thyristor and a substrate having an upper surface, wherein at least one region of the thyristor is in the substrate, the method comprising:

providing a trench having a sidewall in the substrate and adjacent to the thyristor region;

forming a dielectric material on a portion of the sidewall;

forming a control port in the trench, the control port having an uppermost portion recessed below the surface of the substrate and being adapted for capacitively coupling to the thyristor region in the substrate via a portion of the dielectric material extending alongside the control port and below the uppermost portion thereof and for controlling current flow in the thyristor region; and

implanting ions into the substrate without implanting ions into the dielectric material portion extending alongside the control port and below the uppermost portion of the control port.

2. The method of claim 1, wherein the implanting ions into the substrate includes implanting ions to a selected depth below the upper surface of the substrate and wherein forming the control port includes forming the control port recessed at least as low as the selected depth.

3. The method of claim 1, further comprising using a material in the substrate and above the uppermost portion of the control port to inhibit ions from doping the dielectric material portion extending alongside the control port and below the uppermost portion of the control port.

4. The method of claim 3, wherein the using a material in the substrate and above the uppermost portion of the control port includes preventing the dielectric material from being implanted.

5. The method of claim 3, wherein the using a material in the substrate and above the uppermost portion of the control port includes using a filled portion of the trench above the uppermost portion of the control port to inhibit ions from doping the dielectric material portion extending alongside the control port and below the uppermost portion of the control port.

6. The method of claim 1, wherein the implanting ions includes implanting an active region of an adjacent pass device.

7. The method of claim 6, further comprising forming a pass device, wherein the forming a pass device comprises:

ion implanting the active region and a second active region in the substrate adjacent to the trench;

forming a control port over the substrate and between the active regions, the control port being adapted for capacitively coupling to a region in the substrate between the active regions for forming a conductive channel between the active regions; and

electrically coupling the active region to the thyristor.

8. The method of claim 7, further comprising electrically coupling the second active region to a bit line.

9. The method of claim 8, further comprising implanting thyristor body regions in the substrate, one of the body regions including at least a portion of the thyristor region to which the control port is adapted for capacitively coupling.

10. The method of claim 9, wherein the implanting ions into the substrate without implanting ions into the dielectric material portion includes implanting an emitter region above the control port and wherein the electrically coupling the active region to the thyristor includes electrically coupling the active region to the emitter region above the control port.

11. The method of claim 10, wherein the implanting the emitter region and the ion implanting the active region include simultaneously ion implanting the emitter region and the active region.

12. The method of claim 1, wherein the implanting ions into the substrate without implanting ions into the dielectric material portion includes implanting an emitter region of the thyristor.

13. The method of claim 12, wherein the forming the control port includes forming the control port below the emitter region.

14. The method of claim 13, wherein the forming the control port includes forming a control port that is configured and arranged for capacitively coupling to the thyristor region in the substrate for controlling current flow in the thyristor without capacitively coupling to the emitter region.

15. The method of claim 13, further comprising forming the thyristor in the substrate adjacent to the trench, a portion of the thyristor including the thyristor region that the control port is adapted for capacitively coupling to, wherein the forming the thyristor includes ion implanting the emitter region immediately adjacent to the thyristor region that the control port is adapted for capacitively coupling to, wherein the control port is recessed sufficiently below the emitter region such that ions implanted via the emitter region do not implant the dielectric material extending alongside the control port and below the uppermost portion thereof.

16. The method of claim 1, further comprising electrically coupling the thyristor-based semiconductor device to an array of semiconductor devices and forming a memory array.

17. A method of manufacturing a memory cell having a thyristor electrically coupled in series to a pass device, the method comprising:

etching a trench having a sidewall in a substrate having an upper surface, the trench being etched adjacent to and at least partially around a thyristor region;

forming a buried emitter region of the thyristor in the substrate below and adjacent to the trench;

forming a dielectric material on the sidewall of the etched trench;

forming a control port in the trench and recessed below the upper surface of the substrate;

forming a first base region in the substrate, adjacent to and electrically coupled to the buried emitter region;

implanting a portion of the thyristor region and forming a second base region of the thyristor electrically coupled to the first base region and adapted for capacitively coupling to the control port via the dielectric material;

while using a filled portion of the trench above the uppermost portion of the control port to inhibit ions from doping the dielectric material portion extending alongside the control port and below the uppermost portion of the control port, ion implanting a portion of the substrate and forming a second emitter region of the thyristor

electrically coupled to the second base region and first and second active regions of the pass device; and

forming a gate over the upper surface of the substrate and adapted for controlling current flow between the first and second active regions of the pass device, wherein the pass device and the thyristor form a memory cell adapted for storing information and to effect read and write access to the stored information.